Alternatively, terminal **106** may be connected to a low impedance node—forcing a voltage across element **104**, such that its current may either be measured or used in a circuit. Further, connecting the gate of element **104** to the gate of FET **102** may provide blanking of signal from element **104** whenever FET **102** is off. When FET **102** turns off or transitions to a high-impedance state, element **104** acts in a similar manner—proving useful in circuits where power FET **102** is switched.

Depending upon specific design and performance criteria of a given power transistor, a number of embodiments of the present invention may be provided. In such embodiments, multiple sense elements may be strategically placed throughout a power transistor's structure, in order to—for example—achieve an appropriate gain ratio for the sense element, or obviate thermal and fabrication variations. For example, a number of sense elements may be instantiated throughout a power transistor in a symmetric fashion.

One embodiment of such a configuration is illustrated now with reference to transistor structure **300**, as depicted in FIG. **3**. Transistor **300** is a power FET of the type depicted in FIG. **1***b*. A plurality of sense elements **302** are instantiated in a symmetric fashion throughout transistor **300**.

Operationally, a configuration of the type illustrated in FIG. **3**—where a distributed network of sense elements **302** is gate/source connected to a power FET **300**—may be used in a Kelvin sensing of the drain of FET **300**. A Kelvin sense may be utilized in conjunction with an amplifier to force the drain of the sense elements to be equivalent to the drain of the main FET, and produce a current through the sense elements representative of the total FET current. Such an embodiment may be used in a variety of configurations for sensing voltages throughout a power FET, as well as sensing current.

Thus, the present invention provides a system for optimal matching sense transistor architecture. Various embodiments provide one or more sense transistor elements in central or symmetrically distributed instances throughout a power transistor. In such a manner, any effects of thermal or fabrication variation are minimized or obviated. Various embodiments of the present invention may be readily provided for a variety of current or voltage measurement or sensing applications.

As should be apparent to those of skill in the art, the system of the present invention may be applied in a wide variety of transistor architectures. For example, the present invention may be used to advantage in any semiconductor transistor having a layout topology similar to those illustrated herein. The present invention may be implemented to advantage for PFET and NFET architectures. In all embodiments of the present invention, the constituent constructs, operations, functions or components may be implemented in a wide variety of ways—comprising various suitable circuitry and semiconductor structures. Operational voltage or current levels may be tailored to suit the needs of a particular application. Thus all such variations, and all other similar variations and combinations, are comprehended by the present invention. All such embodiments may be employed to provide the benefits of the present invention.

The embodiments and examples set forth herein are therefore presented to best explain the present invention and enable those skilled in the art to make and utilize the invention. However, those skilled in the art will recognize that the foregoing description and examples have been presented for the purpose of illustration and example only. The teachings and principles of the present invention are applicable to a number of semiconductor device applications. The description as set forth herein is therefore not intended to be exhaustive or to limit the invention to the precise form disclosed. As stated throughout, many modifications and variations are possible in light of the above teaching without departing from the spirit and scope of the following claims.

What is claimed is:

1. A method of producing a sense transistor operatively associated with a power transistor, the method comprising the steps of:

providing a power transistor, having a plurality of alternating source and drain structures, with a plurality of gate structures interposed there between;

at a desired location, forming a sense transistor by providing an isolated portion of either a drain or source structure, wherein the sense transistor has a same local bulk potential as the power transistor; and

coupling some circuitry, external to the power transistor, to the isolated portion.

2. The method of claim **1**, wherein the step of providing a power transistor further comprises providing a power MOSFET.

3. The method of claim **2**, wherein the step of providing a power transistor further comprises providing a power PFET.

4. The method of claim **2**, wherein the step of providing a power transistor further comprises providing a power NFET.

5. The method of claim **1**, wherein the step of forming a sense transistor further comprises providing an isolated portion of a drain structure.

6. The method of claim **1**, wherein the step of forming a sense transistor further comprises providing an isolated portion of a source structure.

7. The method of claim **1**, wherein the step of forming a sense transistor further comprises forming a sense transistor in a central location within the power transistor.

8. The method of claim **1**, wherein the step of forming a sense transistor further comprises forming a plurality of sense transistors in locations symmetrically distributed throughout the power transistor.

9. The method of claim **1**, wherein the step of coupling some circuitry further comprises coupling some current measuring circuitry.

10. The method of claim **1**, wherein the step of coupling some circuitry further comprises coupling some voltage measuring circuitry.

11. A power and sense transistor structure comprising:

a power transistor, having a plurality of alternating source and drain structures, with a plurality of gate structures interposed there between;

a sense transistor having an isolated portion of either a drain or source structure at a desired location within the power transistor, wherein the sense transistor has a same local bulk potential as the power transistor; and

circuitry, external to the power transistor, coupled to the sense transistor.

12. The structure of claim **11**, wherein the power transistor a PFET.

13. The structure of claim **11**, wherein the power transistor comprises an NFET.

14. The structure of claim **11**, wherein the sense transistor is formed by isolating a portion of a drain structure.

15. The structure of claim **11**, wherein the sense transistor is formed by isolating a portion of a source structure.